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for

METHOD FOR FABRICATING THIN FILM TRANSISTORS

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METHOD FOR FABRICATING THIN FILM TRANSISTORS

BACKGROUND

[0001] The present disclosure relates generally to semiconductor device manufacturing, and more particularly to the fabrication methods of thin film transistors used in electro-optical display devices, and the like.

[0002] The manufacture of semiconductor integrated circuits (ICs) and devices require the use of many photolithography process steps to define and create specific circuit components and circuit layouts onto an underlying substrate. Conventional photolithography systems project specific circuit and/or component images, defined by a mask pattern reticle, onto a flat substrate coated with a light sensitive film (photoresist) coating. After image exposure, the film is then developed leaving the printed image of the circuit and/or component on the substrate. The imaged substrate is subsequently processed with techniques such as etching and doping to alter the substrate with the transferred pattern. Photolithography processes are used multiple times during the fabrication of thin film field effect transistors (TFTs) that are used in electro-optical display devices and sensors.

[0003] Each photolithography process sequence represents invested fabrication costs to the final cost of the completed device. Such fabrication costs include all costs related to materials, labor, facilities, production yield losses and the time spent in the production state. Any process flow simplification that provides a reduction in any of the above mentioned cost areas will provide a net improvement to the final cost of fabricating the device. It is highly desirable to create and implement new process flows that feature process simplifications to

lower fabrication costs. The reduction of photolithography process sequences represents a form of process simplification. Such process simplification will provide significant cost improvement for a given production facility to maintain highly competitive cost and output advantages over other manufacturers of similar product devices.

[0004] What is desirable is an improved process flow that features process simplifications to lower fabrication costs while maintaining the required physical and electrical performance characteristics of the semiconductor device and components.

SUMMARY

[0005] A method is disclosed for forming a thin film field effect transistor. On a preliminary substrate having at least a glass substrate layer and a buffer layer, source and drain metal regions of the transistor are formed for defining an opening, in which a silicon layer, gate oxide layer, and gate metal layer are formed thereafter. A first photoresist pattern having a two-portion structure is used for selectively removing portions of the gate metal, gate oxide, and silicon layers. After forming a second photoresist pattern with a coverage area smaller than that of the first photoresist pattern, it is used for reducing the gate metal layer. By doping a predetermined impurity in the silicon layer, a source region and drain region of a predetermined type is completed.

[0006] These and other aspects and advantages will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figs. 1A to 1J illustrate cross-sectional views of a p-channel thin film transistor (P-TFT) going through a conventional production process utilizing six photolithography masks.

[0008] Figs. 2A to 2I illustrate cross-sectional views of a thin film transistor going through a fabrication process utilizing four photolithography masks according to one example of the present disclosure.

[0009] Fig. 3 is a flow diagram summarizing the production process illustrated in Figs. 2A to 2I.

DESCRIPTION

[0010] The present disclosure describes a method for the effective fabrication of thin film field effect transistors (TFTs) using four photolithography masks as opposed to six photolithography masks as used in conventional production flows. The electrically active transistor areas of the final completed TFT devices fabricated in accordance with the present disclosure feature regions and components that are of similar composition and structure as those fabricated by the conventional six mask production flow. For simplifying the illustration, a production process for making a p-channel thin film transistor is used, but it is understood that the process is applicable to n-channel devices as well with appropriate and obvious modifications such as using different doping materials and material compositions.

[0011] Referring now to Figs. 1A through 1J, there are cross-sectional views of the production process sequences of a conventional p-channel thin film transistor (P-TFT) utilizing six photolithography masks. Fig. 1A shows a flat glass substrate 102 initially processed to obtain two additional films stacked upon the substrate surface. A buffer layer 104, usually comprised of an insulating material such as silicon oxide, is either deposited using chemical vapor deposition, or thermally grown in a gaseous environment. A poly-silicon layer 106 is then deposited upon the glass-buffer layer stack. The poly-silicon layer 106 is usually deposited using chemical vapor deposition and may be lightly doped during the deposition process with either n-type or p-type dopants. The optional doping of the poly-silicon layer 106 allows for the adjustment of the TFTs' voltage threshold characteristics along the transistor electrical gate channel that is defined during subsequent steps. It is noted that some conventional flows may use amorphous silicon as the material layer instead of the poly-crystalline silicon layer 106 used in this example.

[0012] The first photolithographic mask pattern 108 is placed on top of the poly-silicon 106, buffer 104, glass substrate 102 stack as shown in Fig. 1B. The mask pattern 108 is used to pattern the poly-silicon regions 106 where transistors will be located on the buffer layer 104 and substrate 102. The poly-silicon regions 106 under the mask pattern 108 are blocked from the poly-silicon etching process, thus forming segregated poly-silicon areas 106 as shown in Fig. 1C, that will subsequently become the base for an individual TFT device or simply TFT. A dielectric layer 110 such as silicon oxide is then either thermally grown in a gaseous environment or deposited by chemical vapor deposition on top of the exposed poly-silicon 106 and buffer 104 areas, as shown in Fig. 1D. This dielectric layer 110 is also known as the gate oxide layer, later serving as the gate

dielectric of the TFT. Fig. 1D also shows the next layer, the gate metal layer 112, deposited on top of the gate oxide layer 110. The gate metal layer 112 is usually deposited upon the gate oxide 110 surface by ion sputtering of a metal source or by a chemical electrolysis process.

[0013] Fig. 1E shows the second photolithography mask pattern 114 situated on top of the gate metal layer 112. This mask pattern 114 allows for the etching-off of selected gate metal areas to create the TFT gate electrodes, as well as gate metal lines horizontal to the substrate 102 plane to connect selected multiple TFT gates forming specific circuit paths. The gate metal etch is usually performed using wet chemistries and may be supplemented with a dry chemical plasma etch.

[0014] Fig. 1F illustrates the view of the gate electrode 112 after the etching of the gate metal layer and after the removal of the mask pattern 114. After the removal of the mask pattern 114, the poly-silicon regions 118 and 120 adjacent to but not directly under the gate electrode 112 are doped with a p-type dopant. This doping process, usually accomplished by ion implantation 116 of p-type dopants such as boron or boron-difluoride, creates the TFTs' P+ source 118 and drain 120 regions within the poly-silicon area 106. It is noted that the poly-silicon region 106 located directly under the gate region, not doped by the doping process becomes the TFTs' electrical gate channel. The active TFT components, source 118, drain 120, gate 112 and transistor channel regions are now complete. It is also noted that the ion implantation process 116 is calibrated such that dopant placement is primarily located within the poly-silicon regions 118 and 120 and the gate metal 112 blocks the doping of the transistor gate channel. For the fabrication of n-channel TFT structures, the source/drain ion

implantation 116 will utilize n-type dopants such as phosphorus to create N+ source and drain regions. A thermal anneal process (not shown in the attached figures) is usually performed after the source, drain doping process to repair any physical damage to the doped layers, as well as to activate and distribute the added dopants.

[0015] Fig. 1G illustrates the cross-sectional view of the TFT device after processing through the third mask. The figure shows an interlevel dielectric (ILD) layer 122 that has been deposited on top of the gate metal 112. The ILD layer 122 has been patterned and etched to create selected areas of vertical openings 124 from the top surface of the ILD layer 122 down to expose the TFT source 118 and drain 120 regions. The ILD layer 122 is usually created by a chemical deposition process and etched using a wet chemical and/or dry chemical plasma process. The vertical openings 124 are then lined and filled with conductive metal(s), usually by ion sputtering, to provide a vertical interconnection path from the top of the ILD layer 122 to the TFTs' source 118 and drain 120 regions.

[0016] After the creation of the filled vertical interconnections, a new blanket metal layer 126 is then deposited upon the ILD layer 122. This metal layer 126 is usually created by ion sputtering of a metal source or by a chemical electrolysis process. The fourth mask pattern (not shown) is then placed on top of the metal layer 126, used to define and create the horizontal metal lines connecting selected source 118 and drain 120 regions of selected TFTs to form a desired circuit. Fig. 1H shows the cross-sectional view of the TFT device after the fourth mask pattern has been applied and the metal pattern etched. The new metal lines 126 on top of the ILD layer 122 are shown connected to the TFT source 118 and drain

120 regions through the previously created and filled vertical interconnects 124. After the formation of the metal lines 126, a passivation dielectric layer 128 is then deposited on top of the TFT device.

[0017] Fig. 1I shows the cross-sectional view of the TFT device after using the fifth mask pattern. The fifth mask pattern has been placed on top of the passivation layer 128 and used to selectively etch off certain regions of the layer to expose a vertical interconnect path opening 130 to the last-placed metal lines 126. The etched openings 130 are vertical interconnection paths to connect the last-placed (source and drain) metal lines 126 to the next metal lines that will be created on the top surface of the passivation layer 128. The passivation dielectric layer 128 is usually created by a chemical deposition process and etched using a wet chemical and/or dry chemical plasma process. The vertical openings 130 are lined and filled with conductive metal(s), usually by ion sputtering.

[0018] After the vertical interconnection openings 130 are lined and filled with conductive metal(s), a final routing metal layer 132 is deposited upon the surface of the passivation layer 128. This final conducting layer 132, usually comprised of indium tin oxide (ITO), is then patterned using the sixth and final mask pattern to create the circuit paths for final routing of the TFTs' source 118 and drain 120 regions. Fig. 1J illustrates this showing the filled vertical interconnection openings 130 and the etched ITO metal lines 132. After the completion of this sixth mask processing, the basic TFT device is completed. The basic TFT device features the following basic components, a gate stack comprised of gate electrode metal, gate oxide and an undoped polysilicon region, doped polysilicon regions as the source and drain structures, a first level metal layer for source and drain metal connections and circuit routings, and a second level

metal comprised of ITO for additional source and drain connections and circuit routings.

[0019] Figs. 2A through 2I are cross-sectional views of a p-channel thin film transistor (P-TFT) in production process sequences utilizing four photolithography masks (or mask patterns) in accordance with one example of the present disclosure. Fig. 2A shows a flat glass substrate 202 initially processed to obtain two additional films and the first mask pattern applied upon the stacked substrate surface. Firstly, a buffer layer 204, usually comprised of an insulating material such as silicon oxide, is either deposited using chemical vapor deposition, or thermally grown in a gaseous environment. A metal layer 206 is then deposited upon the glass-buffer stack layer. The metal layer 206 is usually deposited by ion sputtering of a metal source or by a chemical electrolysis process. As shown in Fig. 2A, the first photoresist mask pattern 208 is used to selectively etch and remove areas of the metal layer such that the remaining metal pattern areas define the locations of the TFTs' source and drain metal electrodes as well as the device metal circuit routing of the same. Fig. 2B illustrates the cross-sectional view of the source/drain metal pattern 206 after the completion of the metal pattern and etch process steps.

[0020] The metal patterned, glass-buffer substrate stack 202-206 is then processed through three film additions before the next mask pattern/etch sequence is applied. Fig. 2C shows a poly-silicon layer deposited upon the metal patterned, glass-buffer substrate stack. This poly-silicon (or amorphous silicon) layer 208 is usually deposited using chemical vapor deposition and may be lightly doped during the deposition process with either n-type or p-type dopants. A dielectric layer 210 such as silicon oxide is then either thermally

grown in a gaseous environment or deposited by chemical vapor deposition on top of the poly-silicon 208 layer. This dielectric layer 210 is also known as the gate oxide layer, later serving as the gate dielectric of the TFT device. The next layer, the gate metal layer 212, is deposited on top of the gate oxide layer 210. The gate metal layer 212 is usually deposited upon the gate oxide layer 210 by ion sputtering of a metal source or by a chemical electrolysis process. The second mask photoresist layer 214 is then coated onto selected areas of the gate metal layer 212.

[0021] As shown in Fig. 2C, this second mask pattern may be applied onto selected areas of the gate metal layer 212 as conventional single portion (single height, single width) regions 214. Other selected areas of the gate metal layer 212 may be patterned with portions of the mask of a half-tone mask type having at least two regions on the mask that pass the light at different rates. Because of the light dosage difference, different portions of the photoresist layer are activated to different degrees so that a distinct step-high structure or two-portion structure 214' is formed for each transistor. The two-portion photoresist structure 214' as shown in Fig. 2C features a first portion ***a*** having a predetermined geometry (e.g., height and width). The second portion ***b*** of the photoresist structure underneath ***a*** features a different geometry (e.g., width and height) surrounds the first portion ***a*** to create a two-portion single photoresist structure. It is understood that although ***a*** and ***b*** are referred to as two portions, it is really one photoresist pattern with exactly the same material. The two-portion structure may also be referred to as a step structure as well as one "steps up" from the other. The half-tone masks used can have different designs. It is further understood that for the following illustration, the widths of the first and second portions of the first photoresist pattern are shown as a point of reference to

describe the changes of the layered material for making the TFT, but it is understood that the entire geometry of these layered materials change accordingly. Further, in one example, the half-tone mask has their center region made of a different material than its surrounding region to provide the capabilities for obtaining varied light shielding, thereby imposing varied light exposure dosage in a single exposure process upon the photoresist film. In another example, the two regions of the half-tone masks are made from the same material, but the center region may have a predetermined pattern for blocking or hindering the light from passing through at the same rate as the surrounding region.

[0022] After placement of the second photoresist pattern 214, 214' upon the layered substrate stack 202-212, the non-patterned, exposed areas of the stack as defined by the areas not covered by any photoresist (e.g., both single and two portion structures 214 and 214') are then subjected to etch processes to remove the top three layers: the gate metal 212, gate oxide 210 and poly-silicon 208 layers. Fig. 2D illustrates the view of the device after the etch processes. Typical etch processes used for this stack etch may include wet and dry plasma etch process methods.

[0023] The single portion 214 and two-portion 214' photoresist pattern structures are then selectively reduced to form a second photoresist pattern 215 such that the two-portion structure becomes a single portion structure. The second photoresist pattern has a smaller coverage area (i.e., the area that it covers other materials underneath) than that of the first photoresist pattern 214'. It is noted that the single portion patterns 214 on top of the source and drain metal layers have now been removed along with the removal of portions of the two-

portion photoresist structure. This photoresist pattern removal/reduction can be done by a dry plasma and/or a wet chemical etch process. The residual, new photoresist structure 215 may have its photoresist coverage area as much as or smaller than that of the first portion *a* of the original two-portion structure 214'. Fig. 2E shows the view of the TFT device with the reduced photoresist pattern 215 located on top of the etched stack layer 208-212. The device with the reduced photoresist pattern 215 is then subjected to another etch process for etching only the exposed gate metal layer 212. This etch may be accomplished by using wet chemistry and may be supplemented with a dry chemical plasma etch. The resulting TFT device is shown in Fig. 2F as all previously exposed gate metal layer not covered by the reduced photoresist pattern 215 having been removed. The use of the second mask is now complete and the remaining photoresist 215 is now removed.

[0024] At the completion of this process step, two key transistor definition steps are accomplished. The use of the first photoresist patterns 214 and 214' to etch the gate metal 212, gate oxide 210 and the poly-silicon 208 layers segregates the poly-silicon 208 layer into individual regions (gate stack) for the locations of individual TFTs. The use of the second photoresist pattern 215 to etch the gate metal layer 212 creates the gate electrodes of each TFT. It is noted that by utilizing the single, two-portion photoresist structure 214' significant cost savings can be realized by the provided process simplification comparing to the conventional TFT process flow requiring two separate mask pattern levels to accomplish the two transistor definition steps.

[0025] Fig. 2G illustrates the cross-sectional view of the gate electrode 212 after the removal of the photoresist pattern 215. After removal of the photoresist

pattern 215, the poly-silicon regions 218 and 220 adjacent to, but not directly under the gate electrode 212, are doped with a p-type dopant. This doping process, usually accomplished by ion implantation 216 of p-type dopants such as boron or boron-difluoride, creates the TFTs' P+ source 218 and drains 220 regions within the poly-silicon 208 area. It is noted the poly-silicon region 208 located directly under the gate region, not doped by the doping process becomes the TFTs' electrical gate channel. The active TFT components, source 218, drain 220, gate electrode 212 and transistor channel 208 regions are now completed. It is also noted that the ion implantation process 216 is calibrated such that dopant placement is primarily located within the poly-silicon regions 218 and 220 and that the gate metal 212 blocks the doping of the transistor gate channel 208. For the fabrication of n-channel TFT structures, the source/drain ion implantation 216 will utilize n-type dopants such as phosphorus to create N+ source and drain regions 218, 220. A thermal anneal process (not shown in the attached figures) is usually performed after the source, drain doping process to repair any physical damage to the doped layers, as well as to activate and distribute the added dopants.

[0026] Fig. 2H illustrates the cross-sectional view of the TFT device after processing through the third mask pattern. Fig. 2H shows an ILD, or interlevel dielectric (or dielectric passivation) layer 222 deposited on top of the gate metal 212 and the gate oxide layer 210 after the creation of the doped TFT source 218 and drain 220 regions. The ILD layer 222 has been patterned and etched to create selected areas of vertical openings 224 from the top surface of the ILD layer 222 to expose the TFT source 218 and drain 220 regions and portions of the source and drain metal electrode regions 206. The ILD layer 222 is usually created by a

chemical deposition process and etched using a wet chemical and/or dry chemical plasma process.

[0027] Referring now to Fig. 2I, the vertical openings 224 of fig 2H are then lined and filled with conductive metal(s), usually by ion sputtering, to provide vertical interconnection paths from the top of the ILD layer 222, to the TFTs' source 218 and drain 220 regions and to the source and drain metal electrode regions 206. After the creation of the filled vertical interconnections, a new blanket metal layer 226 is then deposited upon the ILD layer 222 and the filled vertical openings 224. This final metal layer 226 is typically comprised of indium tin oxide (ITO), usually created by ion sputtering of a metal source or by a chemical electrolysis process. It is this ITO metal layer 226 and the filled vertical interconnections by which the source and drain metal lines and areas 206 are connected to the TFT source 218 and drain 220 regions.

[0028] The last (fourth) mask process is then used to define and create the horizontal metal lines for final connection of the TFTs and definition of the desired device circuits. Fig. 2I shows the view of the TFT device after the fourth mask has been applied and the ITO layer patterned and etched. The ITO metal lines 226 defined on top of the ILD layer 222 are shown connected to the TFT source 218 and drain 220 regions through the previously created and filled vertical interconnects 224.

[0029] At this point, the basic TFT device is completed by using only four masks in the manufacturing process. The basic TFT device, just as produced by the conventional 6 mask fabrication processes, features the same basic components, a gate stack comprised of gate electrode metal, gate oxide and an undoped polysilicon region, doped polysilicon regions as the source and drain

structures, a first level metal layer for source and drain metal connections and circuit routings, and a second level metal comprised of ITO for additional source and drain connections and circuit routings.

[0030] Fig. 3 is a flow diagram 300 summarizing the purpose and sequence of each photolithography mask process for the above detailed thin film transistor (TFT) fabricated in accordance with the present disclosure. In step 302, the first mask is used to create the TFTs' source and drain metal electrodes, as well as the first level of device metal circuit routes upon the glass substrate and buffer layers. The second mask pattern step 304 allows for multiple etch processes to be performed using a single photoresist pattern process. The process patterns and etches the poly-silicon, gate oxide and the gate metal layers to create the individual locations for each TFT using a two-portion structure of a photoresist pattern in a single exposure process. The use of only one mask to formulate the gate metal layer and the poly-silicon, gate oxide layers with different widths reduces manufacturing cost for making such a TFT device. In step 306, the process patterns and etches a dielectric layer to create vertical openings for interlevel connections between the TFTs' source and drain regions, the source and drain metal electrodes and the next metal layer. Metal connections are then made between the source and drain regions and the source and drain electrode lines as well as an overlaying metal circuit layer placed on top. In step 308, the process patterns the final overlaying metal layer, usually comprised of ITO material, to create final specific circuit routes with connections to the TFT's source and drain regions.

[0031] The completed TFT device as fabricated in accordance with the present disclosure is accomplished with the use of only four photolithographic masks.

The TFT devices' physical dimensions, material compositions, and component locations are similar as those produced by the conventional fabrication flows utilizing six photoresist masks, to provide similar device electrical behavior and performance. The present disclosure allows for the process simplification of the TFT fabrication, by the creation of the source and drain metal layers first and then by allowing a single mask to be used to accomplish the tasks of several conventional masks. The reduction of photolithography processes provided by the present disclosure results with process simplifications that will translate into significant cost improvements for a given production facility to maintain highly competitive cost and output advantages over other manufacturers of similar product devices.

[0032] The method disclosed is suitable and compatible for implementation within existing, conventional and future fabrication process technologies. The above disclosure provides several examples for implementing the different features of the disclosure. Specific examples of components and processes are described to help clarify the disclosure. These are, of course, merely examples and are not intended to limit the scope of the disclosure from that described in the claims.

[0033] While the invention has been particularly shown and described with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention, as set forth in the following claims.